

EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 58053090
 PUBLICATION DATE : 29-03-83

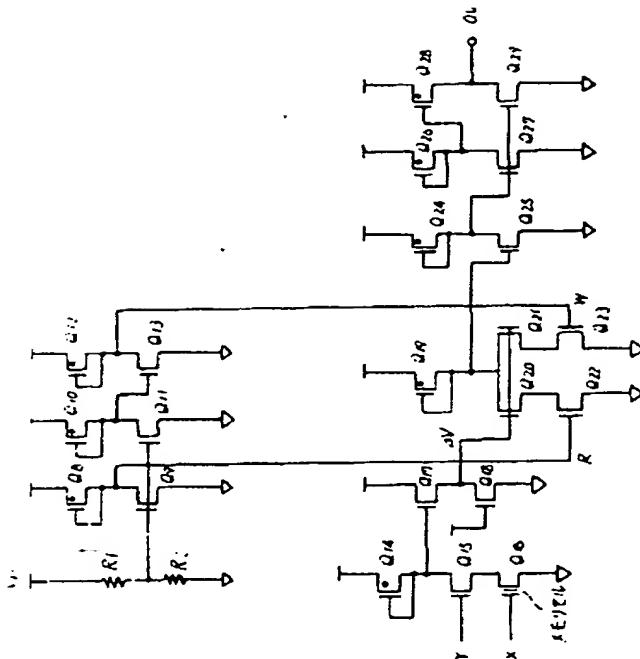
APPLICATION DATE : 24-09-81
 APPLICATION NUMBER : 56151032

APPLICANT : FUJITSU LTD;

INVENTOR : NAKANO RIKIZO;

INT.CL. : G11C 17/00

TITLE : PROGRAMMABLE READ ONLY
 MEMORY



ABSTRACT : PURPOSE: To easily detect defective bits at room temperature in a short time, by selecting threshold values different between the normal operation mode and each test modes, and reading out the memory content.

CONSTITUTION: A MOS transistor (TR) Q₁₆ out of TRs Q₈~Q₂₉ has a floating gate. Through the resistor ratio of R₁ to R₂, a gate voltage in turning Q₉, Q₁₁ off at V_p=5V and that turning on the Q₉, Q₁₁ at V_p=25V at test are produced. Normally, the readout from a memory cell is determined with the threshold value of the Q₂₀, and the sense output is outputted to an output terminal OUT via the Q₂₅, Q₂₇ and Q₂₉. At test, the readout from the memory cell is determined with the threshold value of the Q₂₁ and the sense output is outputted to an output terminal OUT via the Q₂₅, Q₂₇ and Q₂₉.

COPYRIGHT: (C) JPO